Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

1) – 8) (cancelled)

9) (previously presented): A circuit, comprising:

a first node capable to provide a first variable voltage;

a second node capable to provide a second variable voltage;

a first transistor, coupled to the first node, having a first gate capable to provide a first current responsive to a first control voltage being applied to the first gate;

a second transistor, coupled to the second node, having a second gate capable to provide a second current responsive to a second control voltage being applied to the second gate;

a third transistor, coupled to the first node, having a third gate coupled to the first node, capable to provide a third current responsive to the first variable voltage;

a fourth transistor, coupled to the second node, having a fourth gate coupled to the second node, capable to provide a fourth current responsive to the second variable voltage;

a first control circuit, coupled to the first gate and the second node, capable to provide the first control voltage responsive to the second variable voltage; and,

a second control circuit, coupled to the second gate and the first node, capable to provide the second control voltage responsive to the first variable voltage,

wherein the first transistor, the second transistor, the third transistor and the fourth transistor are n-type transistors.

10) (previously presented): A circuit, comprising:

a first node capable to provide a first variable voltage;

a second node capable to provide a second variable voltage;

a first transistor, coupled to the first node, having a first gate capable to provide a first current responsive to a first control voltage being applied to the first gate;

a second transistor, coupled to the second node, having a second gate capable to provide a

second current responsive to a second control voltage being applied to the second gate;

a first control circuit, coupled to the first gate and the second node, capable to provide the first control voltage responsive to the second variable voltage;

a second control circuit, coupled to the second gate and the first node, capable to provide the second control voltage responsive to the first variable voltage;

a third transistor, coupled to the first node, having a third gate coupled to the first node, capable to provide a third current responsive to the first variable voltage;

a fourth transistor, coupled to the second node, having a fourth gate coupled to the second node, capable to provide a fourth current responsive to the second variable voltage;

wherein the first control circuit includes,

a voltage source;

a fifth transistor, coupled to the voltage source, having a gate;

a sixth transistor, coupled to the fifth transistor, having a gate coupled to the first transistor gate;

a seventh transistor, coupled to the voltage source, having a gate; and,

an eighth transistor, coupled to the seventh transistor, having a gate coupled to the second node.

11) (previously presented): A circuit, comprising:

a first node capable to provide a first variable voltage;

a second node capable to provide a second variable voltage;

a first transistor, coupled to the first node, having a first gate capable to provide a first current responsive to a first control voltage being applied to the first gate;

a second transistor, coupled to the second node, having a second gate capable to provide a second current responsive to a second control voltage being applied to the second gate;

a first control circuit, coupled to the first gate and the second node, capable to provide the first control voltage responsive to the second variable voltage;

a second control circuit, coupled to the second gate and the first node, capable to provide the second control voltage responsive to the first variable voltage;

a third transistor, coupled to the first node, having a third gate coupled to the first node,

capable to provide a third current responsive to the first variable voltage;

a fourth transistor, coupled to the second node, having a fourth gate coupled to the second node, capable to provide a fourth current responsive to the second variable voltage;

wherein the first control circuit includes,

a voltage source;

a fifth transistor, coupled to the voltage source, having a gate;

a sixth transistor, coupled to the fifth transistor, having a gate coupled to the first transistor gate;

a seventh transistor, coupled to the voltage source, having a gate;

an eighth transistor, coupled to the seventh transistor, having a gate coupled to the second node;

wherein the second control circuit includes,

a ninth transistor coupled to the voltage source;

a tenth transistor, coupled to the ninth transistor, having a gate coupled to the first node;

an eleventh transistor coupled to the voltage source; and,

a twelfth transistor, coupled to the eleventh transistor, having a gate coupled to the second transistor gate.

12) (previously presented): The circuit of claim 11, wherein the circuit is a cross-coupled load with a built-in current mirrors circuit used in a double data rate receiving circuit for improving a clock signal.

13) (previously presented): The circuit of claim 11, wherein the circuit is in a memory device.

14) (previously presented): The circuit of claim 11, wherein the circuit is in a memory device controller.

15) - 18) (cancelled)

19) (previously presented): A circuit for correcting a duty cycle of a clock signal, comprising:

a first node capable to provide a first variable voltage representing the clock signal;

a second node capable to provide a second variable voltage representing the clock signal;

a first transistor, coupled to the first node, having a first gate capable to provide a first current responsive to a first control voltage being applied to the first gate, wherein the first transistor is operating in a saturation region;

a second transistor, coupled to the second node, having a second gate capable to provide a second current responsive to a second control voltage being applied to the second gate, wherein the second transistor is operating in a saturation region;

a first control circuit, coupled to the first gate and the second node, capable to provide the first control voltage responsive to the second variable voltage;

a second control circuit, coupled to the second gate and the first node, capable to provide the second control voltage responsive to the first variable voltage, wherein the first variable voltage is greater than the second variable voltage;

a third transistor, coupled to the first node, having a third gate coupled to the first node, capable to provide a third current responsive to the first variable voltage;

a fourth transistor, coupled to the second node, having a fourth gate coupled to the second node, capable to provide a fourth current responsive to the second variable voltage;

wherein the first control circuit includes:

a voltage source;

a fifth transistor, coupled to the voltage source, having a gate;

a sixth transistor, coupled to the fifth transistor, having a gate coupled to the first transistor gate;

a seventh transistor, coupled to the voltage source, having a gate; and,

an eighth transistor, coupled to the seventh transistor, having a gate coupled to the second node.

20) (previously presented): A circuit for correcting a duty cycle of a clock signal, comprising:

a first node capable to provide a first variable voltage representing the clock signal;

a second node capable to provide a second variable voltage representing the clock signal;

a first transistor, coupled to the first node, having a first gate capable to provide a first current responsive to a first control voltage being applied to the first gate, wherein the first transistor is operating in a saturation region;

a second transistor, coupled to the second node, having a second gate capable to provide a second current responsive to a second control voltage being applied to the second gate, wherein the second transistor is operating in a saturation region;

a first control circuit, coupled to the first gate and the second node, capable to provide the first control voltage responsive to the second variable voltage;

a second control circuit, coupled to the second gate and the first node, capable to provide the second control voltage responsive to the first variable voltage, wherein the first variable voltage is greater than the second variable voltage;

a third transistor, coupled to the first node, having a third gate coupled to the first node, capable to provide a third current responsive to the first variable voltage;

a fourth transistor, coupled to the second node, having a fourth gate coupled to the second node, capable to provide a fourth current responsive to the second variable voltage;

wherein the first control circuit includes:

a voltage source;

a fifth transistor, coupled to the voltage source, having a gate;

a sixth transistor, coupled to the fifth transistor, having a gate coupled to the first transistor gate;

a seventh transistor, coupled to the voltage source, having a gate;

an eighth transistor, coupled to the seventh transistor, having a gate coupled to the second node;

wherein the second control circuit includes,

a ninth transistor coupled to the voltage source;

a tenth transistor, coupled to the ninth transistor, having a gate coupled to the first node;

an eleventh transistor coupled to the voltage source; and,

a twelfth transistor, coupled to the eleventh transistor, having a gate coupled to the second transistor gate.

21) - 23) (cancelled)

24) (previously presented): An apparatus, comprising:

a transmit circuit capable to transmit serial data; and,

a receive circuit, coupled to the transmit circuit, capable to generate an output signal responsive to the serial data, wherein the receive circuit includes,

a first node capable to provide a first variable voltage;

a second node capable to provide a second variable voltage;

a first transistor, coupled to the first node, having a first gate capable to provide a first current responsive to a first control voltage being applied to the first gate;

a second transistor, coupled to the second node, having a second gate capable to provide a second current responsive to a second control voltage being applied to the second gate;

a first control circuit, coupled to the first gate and the second node, capable to provide the first control voltage responsive to the second variable voltage;

a second control circuit, coupled to the second gate and the first node, capable to provide the second control voltage responsive to the first variable voltage;

a third transistor, coupled to the first node, having a third gate coupled to the first node, capable to provide a third current responsive to the first variable voltage;

a fourth transistor, coupled to the second node, having a fourth gate coupled to the second node, capable to provide a fourth current responsive to the second variable voltage;

wherein the first control circuit includes,

a voltage source;

a fifth transistor, coupled to the voltage source, having a gate;

a sixth transistor, coupled to the fifth transistor, having a gate coupled to the first

transistor gate;

a seventh transistor, coupled to the voltage source, having a gate; and,

an eighth transistor, coupled to the seventh transistor, having a gate coupled to the second node.

25) (previously presented): An apparatus, comprising:

a transmit circuit capable to transmit serial data; and,

a receive circuit, coupled to the transmit circuit, capable to generate an output signal responsive to the serial data, wherein the receive circuit includes,

a first node capable to provide a first variable voltage;

a second node capable to provide a second variable voltage;

a first transistor, coupled to the first node, having a first gate capable to provide a first current responsive to a first control voltage being applied to the first gate;

a second transistor, coupled to the second node, having a second gate capable to provide a second current responsive to a second control voltage being applied to the second gate;

a first control circuit, coupled to the first gate and the second node, capable to provide the first control voltage responsive to the second variable voltage;

a second control circuit, coupled to the second gate and the first node, capable to provide the second control voltage responsive to the first variable voltage;

a third transistor, coupled to the first node, having a third gate coupled to the first node, capable to provide a third current responsive to the first variable voltage;

a fourth transistor, coupled to the second node, having a fourth gate coupled to the second node, capable to provide a fourth current responsive to the second variable voltage;

wherein the first control circuit includes,

a voltage source;

a fifth transistor, coupled to the voltage source, having a gate;

a sixth transistor, coupled to the fifth transistor, having a gate coupled to the first

transistor gate;

a seventh transistor, coupled to the voltage source, having a gate;

an eighth transistor, coupled to the seventh transistor, having a gate coupled to the second node;

wherein the second control circuit includes,

a ninth transistor coupled to the voltage source;

a tenth transistor, coupled to the ninth transistor, having a gate coupled to the first node;

an eleventh transistor coupled to the voltage source; and,

a twelfth transistor, coupled to the eleventh transistor, having a gate coupled to the second transistor gate.

26) (previously presented): The apparatus of claim 25, wherein the transmit circuit is included in a memory controller and the receive circuit is included in a memory device.

27) (previously presented):The apparatus of claim 25, wherein the receive circuit is a circuit used for improving a clock signal.

28) – 31) (cancelled)